CLAIMS

1. An electronic device having a clock generation circuit, the clock generation circuit comprising:

a) a phase locked loop generating a control signal and having a clock output and an enable input enabling operation of the phase locked loop when a first value is applied to the enable input and disabling the phase locked loop when a second value is applied to the enable input, and;

b) a control circuit having an output connected to the enable input, the control circuit comprising:

i) a first sub-circuit, receiving the control signal and producing an output indicating the condition of the control signal;

ii) a second sub-circuit, coupled to the clock output of the phase locked loop, that detects a pulse and produces an output indicating that a pulse is present during a first interval of time; and

iii) a third sub-circuit, having inputs coupled to the first sub-circuit and the second sub-circuit and an enable output, the third sub-circuit, when at least one of the control voltage and the pulse are not detected at the end of the first interval of time, provides an enable input to the phase locked loop with the second value and maintains the enable input with the second value for a second interval of time and thereafter provides the enable input the first value for at least a third interval of time.

2. The electronic device of claim 1 wherein the output of the second sub-circuit indicates a pulse when the second sub-circuit detects both a rising edge in the clock input and a falling edge during the first interval of time.

3. The electronic device of claim 1 additionally comprising a oscillator, and the first interval is defined by counting a predetermined number of oscillations of the oscillator.

4. The electronic device of claim 1 wherein the first sub-circuit produces an output indicating the control signal exceeds a predetermined threshold.

5. The electronic device of claim 1 wherein the third sub-circuit provides an output signal termed the stable output, with a value indicating the phase locked loop is settled when, at the end of the first interval, both the control voltage and the pulse are detected.

6. The electronic device of claim 5 additionally comprising a microprocessor core having a control input, the enable input of the microprocessor core coupled to the stable output of the third sub-circuit, the microprocessor core being enabled in response to the control input having the value indicating the phase locked loop is settled.

7. The electronic device of claim 5 wherein the third sub-circuit provides the stable output with a value indicating the phase locked loop is settled when the pulse and the control voltage are detected concurrently.

8. The electronic device of claim 1 wherein the first sub-circuit comprises an analog comparator.

9. The electronic device of claim 8 wherein the second sub-circuit consists essentially of digital logic.

10. The electronic circuitry of claim 9 wherein the second sub-circuit comprises a flip-flop having two edge triggered inputs coupled to the output of the phase locked loop, with one of said inputs being the logical inverse of the other of said inputs.

11. The electronic device of claim 1 additionally comprising a fixed oscillator and a fourth sub-circuit having an input coupled to the supply voltage for the phase locked loop and an output indicating that a predetermined time has passed since the supply voltage exceed a threshold.

12. A method of operating a timing circuit having a phase locked loop, the method comprising:

a) during a first interval, checking whether a control signal in the phase locked loop is between a maximum allowed value and a minimum allowed value;

b) when the control signal in the phase locked loop is above a maximum allowed value or below a minimum allowed value, disabling the phase locked loop for a second interval; and

c) when the control signal in the phase locked loop is below a maximum allowed value and above a minimum allowed value, indicating that the output of the phase locked loop is stable.

13. The method of operating a timing circuit having a phase locked loop of claim 12 wherein checking whether the control signal in the phase locked loop is between a maximum allowed value and a minimum allowed value comprises:

a) comparing the control signal to a threshold representing the minimum allowed value; and

b) detecting an oscillation at the output of the phase locked loop.

14. The method of operating a timing circuit having a phase locked loop of claim 13 wherein detecting an oscillation comprises using digital logic circuitry to detect at least one pulse during the first interval.

15. The method of operating a timing circuit having a phase locked loop of claim 12 additionally comprising, after the second interval, re-enabling the phase locked loop and repeating the method of claim 12.

16. The method of operating a timing circuit having a phase locked loop of claim 15 additionally comprising, iteratively repeating the method of claim 15 until the output is indicated to be stable.

17. The method of operating a timing circuit having a phase locked loop of claim 12 wherein the timing circuit is part of an electronic device having a microprocessor core and the method further comprises selectively enabling the microprocessor core in response to an indication that the phase locked loop is stable.

18. The method of operating a timing circuit having a phase locked loop of claim 12 wherein the phase locked loop comprises a voltage controlled oscillator with a

control input and checking whether the control signal in the phase locked loop is between a maximum allowed value and a minimum allowed value comprises comparing the control input of the voltage controlled oscillator to a threshold.

19. The method of operating a timing circuit having a phase locked loop of claim 12 wherein the first interval and the second interval are determined by counting pulses of an external clock.

20. The method of operating a timing circuit having a phase locked loop of claim 12 wherein the first interval begins a predetermined time after the supply voltage to the phase locked loop exceeds a threshold.

21. A method of operating a timing circuit comprising a phase locked loop comprising:

a) during a first interval, detecting whether a control voltage in the phase locked loop is above a threshold and at least one pulse is produced from the output of the phase locked loop;

b) when the control voltage in the phase locked loop is not above a threshold and at least one pulse is produced from the output of the phase locked loop, disabling the phase locked loop for a second interval;

c) when the control voltage in the phase locked loop is above a threshold and at least one pulse is produced from the output of the phase locked loop, producing an indication that the output of the phase locked loop is stable.

22. The method of operating a timing circuit having a phase locked loop of claim 21 wherein detecting at least one pulse during the first interval comprises using digital circuitry to detect the pulse.

23. The method of operating a timing circuit having a phase locked loop of claim 21 additionally comprising, after the second interval, re-enabling the phase locked loop and repeating the method of claim 21.

24. The method of operating a timing circuit having a phase locked loop of claim 23 additionally comprising, iteratively repeating the method of claim 23 until the output is indicated to be stable.

25. The method of operating a timing circuit having a phase locked loop of claim 21 wherein the timing circuit is part of an electronic device having a microprocessor core and the method further comprises selectively enabling the microprocessor core in response to an indication that the phase locked loop is stable.

26. The method of operating a timing circuit having a phase locked loop of claim 21 wherein the first interval and the second interval are determined by counting pulses of an external clock.

27. The method of operating a timing circuit having a phase locked loop of claim 21 wherein the first interval begins a predetermined time after the supply voltage to the phase locked loop exceeds a threshold.